In the Claims:

Please cancel claims 15, 17, and 18. Please amend claims 1, 4, 7, 12-14, and 20. The claims are as follows:

1. (Currently amended) A plurality of memory arrays, each memory array comprising a compilable address magnitude comparator, the compilable address magnitude comparator of each memory array receiving a self-test address from a self-test controller and comparing the self-test address to a compiled maximum address of ~~the~~ each memory array, the compilable address magnitude comparator of each memory array preventing testing of memory of ~~the~~ each memory array corresponding to the self-test address if the self-test address exceeds the compiled maximum address of each memory array, wherein the compilable address magnitude comparator of each memory array prevents testing of memory of ~~the~~ each memory array by forcing a memory pass signal, wherein the compilable address magnitude comparator of each memory array includes a row comparator and a column comparator, the row comparator comparing a self-test row address of ~~the~~ each memory array and the column comparator comparing a self-test column address of ~~the~~ each memory array, and wherein the compiled maximum address of each memory array comprises a maximum row address of ~~the~~ each memory array and a maximum column address of ~~the~~ each memory array.

2-3. (Canceled)

4. (Currently amended) The memory array of claim 1, wherein the compilable address magnitude comparator of each memory array prevents testing of memory of ~~the~~ each memory array by forcing a read operation instead of a write operation.

5-6. (Canceled)

7. (Currently amended) A plurality of memory arrays, each memory array comprising a compilable address magnitude comparator, the compilable address magnitude comparator of a memory array of the plurality of memory arrays comprising:

a row comparator, the row comparator comparing a row portion of a self-test address from a self-test controller with a compiled maximum row address, the compiled maximum row address corresponding to a maximum valid row address of the memory array; and

a column comparator, the column comparator comparing a column portion of the self-test address with a compiled maximum column address of the memory array, the compiled maximum column address corresponding to a maximum valid column address of the memory array, and wherein the compilable address magnitude comparator modifies a self-test operation of the memory array when either the row portion of the self-test address exceeds the corresponding maximum valid row address of the memory array or the column portion of the self-test address exceeds the corresponding maximum valid column address of the memory array, wherein the compilable address magnitude comparator prevents testing of memory of the memory array by forcing a memory pass signal in a corresponding built-in-self-test controller, wherein the compilable address magnitude comparator prevents testing of memory of the memory array by forcing a read operation instead of a write operation, and wherein the row comparator includes at least one logic block selected from a plurality of logic blocks, with each of the plurality of logic blocks corresponding to a portion of a compiled maximum address of the memory array such that by selecting one of the plurality of logic blocks, the compilable magnitude comparator tests for the compiled maximum address of the memory array.

8-11. (Canceled)

12. (Currently amended) An application specific integrated circuit, the application specific integrated circuit comprising:

a plurality of memory arrays, each memory array comprising a compilable address magnitude comparator;

a built-in-self-test controller coupled to each memory array , the built-in-self-test controller testing the memory of each memory array, the compilable address magnitude comparator in each memory array receiving a self-test address from the built-in-self-test controller and comparing the received self-test address with a compiled maximum address of the each memory array, wherein the compiled maximum address of each memory array corresponds to the highest valid address for the each memory array, and wherein the compilable address magnitude comparator of each memory array prevents the built-in-self-test controller from testing a memory location of the each memory array corresponding to the self-test address if the self-test address exceeds the compiled maximum address of each memory array, wherein the compilable address magnitude comparator of each memory array prevents testing of memory of each memory array by forcing a read operation instead of a write operation, and wherein the compilable address magnitude comparator of each memory array prevents testing of memory of each memory array by further forcing a memory pass signal, and wherein ~~the~~ a second memory array of the plurality of memory arrays has a different maximum number of columns than does ~~the~~ a first memory array of the plurality of memory arrays.

13. (Currently amended) The application specific integrated circuit of claim , wherein the compilable address magnitude comparator of each memory array includes a row comparator and a column comparator, the row comparator of each memory array comparing a self-test row address and the column comparator of each memory array comparing a self-test column address.

14. (Currently amended) The application specific integrated circuit of claim ~~13~~ 12, wherein the compiled maximum address of each memory array comprises a maximum row address of ~~the~~ each memory array and a maximum column address of ~~the~~ each memory array.

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Currently amended) The application specific integrated circuit of claim 12, wherein the comparator of each memory array is compilable by selectively substituting a plurality of compilable logic blocks according to the compiled maximum address of each memory array.